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EXAMINER	
ORTIZ, EDGARDO	

ART UNIT	PAPER NUMBER
2815	

DATE MAILED: 06/29/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/091,795	MOSLEHI, MEHRDAD M.	
	Examin r	Art Unit	
	Edgardo Ortiz	2815	

-- The MAILING DATE of this communication appears n the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *06 March 2002*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1 and 51-84* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☐ Claim(s) *1 and 51-84* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *March 6, 2002*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Double Patenting

1. A rejection based on double patenting of the "same invention" type finds its support in the language of 35 U.S.C. 101 which states that "whoever invents or discovers any new and useful process ... may obtain a patent therefor ..." (Emphasis added). Thus, the term "same invention," in this context, means an invention drawn to identical subject matter. See *Miller v. Eagle Mfg. Co.*, 151 U.S. 186 (1894); *In re Ockert*, 245 F.2d 467, 114 USPQ 330 (CCPA 1957); and *In re Vogel*, 422 F.2d 438, 164 USPQ 619 (CCPA 1970).

A statutory type (35 U.S.C. 101) double patenting rejection can be overcome by canceling or amending the conflicting claims so they are no longer coextensive in scope. The filing of a terminal disclaimer cannot overcome a double patenting rejection based upon 35 U.S.C. 101.

Claim 1 is rejected under 35 U.S.C. 101 as claiming the same invention as that of claim 1 of prior U.S. Patent No. 6,016,000. This is a double patenting rejection.

Claim Rejections - 35 USC § 102

2. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

Claims 1, 64, 67, 78 and 79 are rejected under 35 U.S.C. 102(e) as being anticipated by Singh et al. (U.S. Patent No. 5,960,311). With regard to Claim 1, Singh discloses a plurality of electrically conductive metallization levels (column 4, line 61 and figure 3b), each of said metallization

levels comprising a plurality of electrically conductive interconnect segments (48, 50, 52, 54, 56, 58 and 59), a plurality of electrically conductive plugs (43a-43d) for electrically connecting between various metallization levels and between said metallization levels and a plurality of semiconductor devices, a free-space medium (70, 72) occupying at least a substantial portion of the electrically insulating regions (46) within said multi-level interconnect structure and an electrically insulating top passivation overlayer (80).

The limitation *"for hermetic sealing of said multi-level interconnect structure and for protection of said integrated circuit chip, said top passivation overlayer also serving as a heat transfer medium for facilitating heat removal from said interconnect structure and providing additional mechanical support for said interconnect structure through contact with the top metallization level"*, is an intended use limitation that does not distinguish the claimed structure from that disclosed by the cited prior art.

With regard to Claim 64, Singh discloses at least one metallization level (column 4, lines 61 and figure 3b), a first insulating layer (46) overlying sad at least one metallization level, wherein said first insulating includes a plurality of openings, a free-space dielectric medium (70, 72) surrounding a portion of said at least one metallization level, a conformal insulating layer, which is the region of (46) underneath the free-space dielectric medium, between said at least one metallization level and said free-space dielectric medium and a non-conformal insulating layer (84) that seals the openings.

With regard to Claim 67, Singh discloses a first metallization level comprising a plurality of electrically conductive interconnect segments (48, 50, 52, 54, 56, 58 and 59) and a second metallization level comprising a plurality of electrically conductive interconnect segments (48', 50', 52', 54', 56', 58' and 59') overlying said first metallization level, wherein said second metallization level does not utilize any electrically conductive diffusion barrier layer.

With regard to Claim 78, Singh discloses at least one metallization level comprising, a first metallization level comprising a plurality of electrically conductive interconnect segments (48, 50, 52, 54, 56, 58 and 59) and a second metallization level comprising a plurality of electrically conductive interconnect segments (48', 50', 52', 54', 56', 58' and 59') overlying said first metallization level, wherein said second metallization level does not utilize any electrically conductive diffusion barrier layer, a first insulating layer (46) overlying sad at least one metallization level, wherein said first insulating includes a plurality of openings, a free-space dielectric medium (70, 72) surrounding a portion of said at least one metallization level, an electrically insulating layer (84) that seals the openings.

With regard to Claim 79, Singh discloses a conformal insulating layer, which is the region of (46) underneath the free-space dielectric medium (70, 72), between said at least one metallization level and said free-space dielectric medium and a non-conformal insulating layer (84) that seals the openings.

Claim Rejections - 35 USC § 103

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 51-63, 65, 66, 68-77 and 80-84 are rejected under 35 U.S.C. 103(a) as being unpatentable over Singh et al. (U.S. Patent No. 5,960,311) in view of Hause et al. (U.S. Patent No. 6,091,149). With regard to Claim 51, Singh discloses at least one metallization level (column 4, lines 61 and figure 3b), a first insulating layer (46) overlying sad at least one metallization level, wherein said first insulating includes a plurality of openings, a free-space dielectric medium (70, 72) surrounding a portion of said at least one metallization level, and an electrically insulating layer (80) to hermetically seal said free-space dielectric medium.

However, Singh fails to disclose that the electrically insulating material comprises a first layer and a second layer having a composition different from the first layer and the layers comprising an element selected from a group consisting of nitrogen and carbon. Hause discloses a multi-level interconnect structure including an electrically insulating material sealing a free-space dielectric (see figure 14) comprising a first layer (140) of silicon oxynitride (column 9, line 44) and a second layer (column 10, line 6), wherein the second layer has a composition different (silicon nitride) from the first layer. Therefore, it would have been an obvious to someone with ordinary skill in the art, at the time of the invention, to modify the structure as taught by Singh to include the claimed electrically insulating material comprising a first layer and a second layer

having a composition different from the first layer and the layers comprising an element selected from a group consisting of nitrogen and carbon, as suggested by Hause, in order to provide a protective dual-passivation layer.

With regard to Claim 52, Singh discloses at least one metallization level comprising, a first metallization level comprising a plurality of electrically conductive interconnect segments (48, 50, 52, 54, 56, 58 and 59) and a second metallization level comprising a plurality of electrically conductive interconnect segments (48', 50', 52', 54', 56', 58' and 59') overlying said first metallization level, wherein said second metallization level does not utilize any electrically conductive diffusion barrier layer.

With regard to Claim 53, Singh discloses a bottom insulating buffer layer (44) separating the interconnect structure from underlying transistors and isolation regions (column 4, lines 50-52) within a semiconductor integrated circuit substrate (see figure 3a).

With regard to Claim 54, Singh discloses a bottom insulating buffer layer (44) comprising a diffusion layer (column 5, line 54).

With regard to Claim 55, Singh discloses a free-space medium (70, 72) that comprises gaseous material (column 5, lines 59-61) that occupies at least a substantial fraction of regions between the first metallization level and the second metallization (see figure 3b).

With regard to Claim 56, the claimed pressure range for the gaseous material would have an been obvious modification to the structure as taught by Singh, since it has been held that where the general conditions of a claim are disclosed in the prior art, discovering the optimum or working ranges involves only routine skill in the art. In re Aller, 105 USPQ 233.

With regard to Claim 57, Singh discloses a gaseous material that is at or near atmospheric pressure (column 5, lines 59-61).

With regard to Claim 58, Singh discloses a conformal insulating layer, which is the region of (46) underneath the free-space dielectric medium (70, 72), between said at least one metallization level and said free-space dielectric medium.

With regard to Claim 59, a further difference between the claimed invention and Singh is the electrically insulating material being non-conformal. Hause discloses a multi-level interconnect structure including an electrically insulating material sealing a free-space dielectric (see figure 14) comprising a first layer (140) of silicon oxynitride (column 9, line 44) and a second layer (column 10, line 6), wherein the layers are not conformal. Therefore, it would have been an obvious to someone with ordinary skill in the art, at the time of the invention, to modify the structure as taught by Singh to include the claimed electrically insulating material being non-conformal, as suggested by Hause, in order to provide a protective dual-passivation layer.

With regard to Claim 60, the claimed thickness for the non-conformal layer would have an been obvious modification to the structure as taught by Singh, since it has been held that where the general conditions of a claim are disclosed in the prior art, discovering the optimum or working ranges involves only routine skill in the art. In re Aller, 105 USPQ 233.

With regard to Claim 61, a further difference between the claimed invention and Singh are bonding pad openings. It would have been an obvious to someone with ordinary skill in the art, at the time of the invention, to modify the structure as taught by Singh to include the claimed bond pad openings, in order to provide interconnection to additional layers or structures.

With regard to Claim 62, Singh discloses metallization levels with interconnections (48, 50, 52, 54, 56, 58 and 59) comprising aluminum (column 6, lines 39-41.

With regard to Claim 63, Hause discloses a multi-level interconnect structure including an electrically insulating material sealing a free-space dielectric (see figure 14) comprising a first layer (140) of silicon oxynitride (column 9, line 44) and a second layer (column 10, line 6), wherein the second layer has a composition different (silicon nitride) from the first layer. Therefore, it would have been an obvious to someone with ordinary skill in the art, at the time of the invention, to modify the structure as taught by Singh to include the claimed materials for the second layer, in order to provide a passivation layer using known insulating and protective materials.

With regard to Claim 65, the claimed thickness for the conformal layer would have an been obvious modification to the structure as taught by Singh, since it has been held that where the general conditions of a claim are disclosed in the prior art, discovering the optimum or working ranges involves only routine skill in the art. In re Aller, 105 USPQ 233.

With regard to Claim 66, a further difference between the claimed invention and Singh is the electrically insulating material comprises a first layer and a second layer having a composition different from the first layer and the layers comprising an element selected from a group consisting of nitrogen and carbon. Hause discloses a multi-level interconnect structure including an electrically insulating material sealing a free-space dielectric (see figure 14) comprising a first layer (140) of silicon oxynitride (column 9, line 44) and a second layer (column 10, line 6), wherein the second layer has a composition different (silicon nitride) from the first layer. Therefore, it would have been an obvious to someone with ordinary skill in the art, at the time of the invention, to modify the structure as taught by Singh to include the claimed electrically insulating material comprising a first layer and a second layer having a composition different from the first layer and the layers comprising an element selected from a group consisting of nitrogen and carbon, as suggested by Hause, in order to provide a protective dual-passivation layer.

With regard to Claim 68, Singh discloses at least one metallization level comprising, a first metallization level comprising a plurality of electrically conductive interconnect segments (48, 50, 52, 54, 56, 58 and 59) and a second metallization level comprising a plurality of electrically

conductive interconnect segments (48', 50', 52', 54', 56', 58' and 59') and a free-space medium (70, 72) that comprises gaseous material (column 5, lines 59-61) that occupies at least a substantial fraction of regions between the first metallization level and the second metallization (see figure 3b).

With regard to Claim 69, a further difference between the claimed invention and Singh are the claimed bonding pad openings. It would have been an obvious to someone with ordinary skill in the art, at the time of the invention, to modify the structure as taught by Singh to include the claimed bond pad openings, in order to provide interconnection to additional layers or structures.

With regard to Claim 70, Singh discloses forming at least one metallization level (column 4, lines 61 and figure 3b), forming a free-space dielectric medium (70, 72) surrounding a portion of said at least one metallization level.

However, Singh fails to disclose annealing the at least one metallization level to increase a grain size of at least on metal line within said at least one metallization level . It would have been an obvious to someone with ordinary skill in the art, at the time of the invention, to modify the process as taught by Singh to include the claimed annealing the at least one metallization level to increase a grain size of at least on metal line within said at least one metallization level, since this a well-known process in the semiconductor art in order to enhance electromigration.

With regard to Claim 71, the claimed annealing temperature range would have an been obvious modification to the structure as taught by Singh, since it has been held that where the general conditions of a claim are disclosed in the prior art, discovering the optimum or working ranges involves only routine skill in the art. In re Aller, 105 USPQ 233.

With regard to Claim 72, Singh discloses a conformal insulating layer, which is the region of (46) underneath the free-space dielectric medium (70, 72), between said at least one metallization level and said free-space dielectric medium and a non-conformal insulating layer (84) that seals the openings.

With regard to Claim 73, the claimed thickness for the conformal layer would have an been obvious modification to the structure as taught by Singh, since it has been held that where the general conditions of a claim are disclosed in the prior art, discovering the optimum or working ranges involves only routine skill in the art. In re Aller, 105 USPQ 233.

With regard to Claim 74, a further difference between the claimed invention and Singh is the electrically insulating material comprises a first layer and a second layer having a composition different from the first layer and the layers comprising an element selected from a group consisting of nitrogen and carbon. Hause discloses a multi-level interconnect structure including an electrically insulating material sealing a free-space dielectric (see figure 14) comprising a first layer (140) of silicon oxynitride (column 9, line 44) and a second layer (column 10, line 6), wherein the second layer has a composition different (silicon nitride) from the first layer.

Therefore, it would have been an obvious to someone with ordinary skill in the art, at the time of the invention, to modify the structure as taught by Singh to include the claimed electrically insulating material comprising a first layer and a second layer having a composition different from the first layer and the layers comprising an element selected from a group consisting of nitrogen and carbon, as suggested by Hause, in order to provide a protective dual-passivation layer.

With regard to Claim 75, Singh discloses at least one metallization level comprising, a first metalliation level comprising a plurality of electrically conductive interconnect segments (48, 50, 52, 54, 56, 58 and 59) and a second metallization level comprising a plurality of electrically conductive interconnect segments (48', 50', 52', 54', 56', 58' and 59') overlying said first metallization level, wherein said second metallization level does not utilize any electrically conductive diffusion barrier layer.

With regard to Claim 76, Singh discloses at least one metallization level comprising, a first metallization level comprising a plurality of electrically conductive interconnect segments (48, 50, 52, 54, 56, 58 and 59) and a second metallization level comprising a plurality of electrically conductive interconnect segments (48', 50', 52', 54', 56', 58' and 59') and a free-space medium (70, 72) that comprises gaseous material (column 5, lines 59-61) that occupies at least a substantial fraction of regions between the first metallization level and the second metallization (see figure 3b).

With regard to Claim 77, a further difference between the claimed invention and Singh are the claimed bonding pad openings. It would have been an obvious to someone with ordinary skill in the art, at the time of the invention, to modify the structure as taught by Singh to include the claimed bond pad openings, in order to provide interconnection to additional layers or structures.

With regard to Claim 80, the claimed thickness for the conformal layer would have an been obvious modification to the structure as taught by Singh, since it has been held that where the general conditions of a claim are disclosed in the prior art, discovering the optimum or working ranges involves only routine skill in the art. In re Aller, 105 USPQ 233.

With regard to Claim 81, a further difference between the claimed invention and Singh is the electrically insulating material comprises a first layer and a second layer having a composition different from the first layer and the layers comprising an element selected from a group consisting of nitrogen and carbon. Hause discloses a multi-level interconnect structure including an electrically insulating material sealing a free-space dielectric (see figure 14) comprising a first layer (140) of silicon oxynitride (column 9, line 44) and a second layer (column 10, line 6), wherein the second layer has a composition different (silicon nitride) from the first layer. Therefore, it would have been an obvious to someone with ordinary skill in the art, at the time of the invention, to modify the structure as taught by Singh to include the claimed electrically insulating material comprising a first layer and a second layer having a composition different from the first layer and the layers comprising an element selected from a group consisting of

nitrogen and carbon, as suggested by Hause, in order to provide a protective dual-passivation layer.

With regard to Claim 82, Singh discloses at least one metallization level comprising, a first metallization level comprising a plurality of electrically conductive interconnect segments (48, 50, 52, 54, 56, 58 and 59) and a second metallization level comprising a plurality of electrically conductive interconnect segments (48', 50', 52', 54', 56', 58' and 59') and a free-space medium (70, 72) that comprises gaseous materal (column 5, lines 59-61) that occupies at least a substantial fraction of regions between the first metallization level and the second metallization (see figure 3b).

With regard to Claim 83, a further difference between the claimed invention and Singh are the claimed bonding pad openings. It would have been an obvious to someone with ordinary skill in the art, at the time of the invention, to modify the structure as taught by Singh to include the claimed bond pad openings, in order to provide interconnection to additional layers or structures.

With regard to Claim 84, Singh discloses a second metallization level that comprises an adhesion layer (80).

Conclusion

4. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Edgardo Ortiz whose telephone number is 571-272-1735. The examiner can normally be reached on Monday-Friday (1st Friday Off).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Tom Thomas can be reached on 571-272-1664. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

ALLAN R. WILSON
PRIMARY EXAMINER

E.O.
A.U. 2815
6/27/04